REMARKS

In the last Office Action, claims 15-16 were rejected under 35 U.S.C. §102(b) as being anticipated by Wen-Shiung Lour and Chung-Cheng Chang in Solid States Electronics, vol. 39, issue 9, pp. 1295-1298 (1986) ("Wen"). The Examiner contends that Wen discloses each and every element of the photodiode recited in claims 15-16. Claims 1-7 were rejected under 35 U.S.C. §103(a) as being unpatentable over Wen in view of applicant's prior art disclosure in Figs. 2 and 3 ("APD"). The Examiner contends that the subject matter of claims 1-7 is taught by the combined teachings of Wen and APD. Applicant respectfully traverses the prior art rejections of claims 1-7 and 15-16 and requests reconsideration of his application in light of the following discussion.

Brief Summary of the Invention

The present invention is directed to a short-wavelength photodiode of enhanced sensitivity with low leak current.

As described in the specification (pgs. 1-3), the detection of light sensitivity in a short wavelength region by conventional photodiodes is inferior. Furthermore, the conventional photodiodes are associated with high leak current.

The present invention overcomes the drawbacks of the conventional art. Fig. 1 shows a photodiode according to the present invention embodied in independent claim 1.
The photodiode comprises an optical detection portion for detecting an optical signal and outputting a photoelectric conversion signal. The optical detection portion has a semiconductor substrate 1 of a first conductive type and semiconductor layers 2a, 2b of a second conductive type formed in spaced-apart relation in a surface of the semiconductor substrate. A depletion layer 3 is formed in the semiconductor substrate 1 by application of a reverse bias to the photodiode so as to surround the semiconductor layers 2a, 2b. An etched surface portion (denoted by X in the copy of Fig. 1 submitted herewith as Exhibit A) of the depletion layer 3 is disposed between the semiconductor layers 2a, 2b so that an interface level region of the surface of the semiconductor substrate 1 does not exist between the semiconductor layers 2a, 2b.

By the foregoing photodiode construction, the present invention provides a short-wavelength photodiode of enhanced sensitivity and with low leak current. By etching the surface portion of the depletion layer which is disposed between the semiconductor layers so that the interface level region of the surface of the semiconductor substrate does not exist between the semiconductor layers, leak current is

controlled without greatly influencing the photo sensitivity of the photodiode.

The prior art of record does not disclose or suggest the subject matter recited in independent claims 1 and 15 and dependent claims 2-7 and 16.

Traversal of Prior Art Rejections

Rejection Under 35 U.S.C. §102(b)

Claims 15-16 were rejected under 35 U.S.C. §102(b) as being anticipated by Wen. Applicant respectfully traverses this rejection and submits that claims 15-16 recite subject matter which is not disclosed or described by Wen.

Independent claim 15 is directed to a photodiode and requires an optical detection portion for detecting an optical signal and outputting a photoelectric conversion signal, the optical detection portion having a semiconductor substrate of a first conductive type and a plurality of semiconductor layers of a second conductive type disposed in spaced-apart relation in a surface of the semiconductor substrate so that an interface level region of the surface of the semiconductor substrate does not exist between the semiconductor layers. No corresponding structural combination is disclosed or suggested by the prior art of record.

Wen discloses a PIN photodiode. With reference to Fig. 1 of Wen which has been reproduced herewith as Exhibit B, the PIN photodiode has a P-Si substrate (corresponding to the semiconductor substrate of the claimed invention), an n-type ZnSe layer (corresponding to the semiconductor layers in the claimed invention) formed on the P-Si substrate, and two n+ layers spaced-apart from one another and disposed on the n-type ZnSe layer. The n+ layers are employed as ohmic contacts for the n-type ZnSe layer and an electrode formed on the n+ layers. The n+ layers have an etched surface portion for the purpose of forming an electrode pattern and removing a light obstacle. A depletion layer is formed in the n-type ZnSe layer above the P-Si substrate.

In the statement of rejection, the Examiner contends that the P-Si substrate and the n-type ZnSe layer in Wen correspond to the semiconductor substrate in independent claim 15 and that the n+ layers (i.e., ohmic contacts) correspond to the semiconductor layers in independent claim 15. Applicant respectfully disagrees with the Examiner's contentions and with the Examiner's interpretation of Wen in the rejection of the claims.

Wen does not disclose or describe a plurality of semiconductor layers disposed in spaced-apart relation in a surface of the semiconductor substrate so that an interface

level region of the surface of the s miconductor substrate does not exist between the semiconductor layers, as required by independent claim 15. Contrary to the Examiner's contention, one of ordinary skill in the art would recognize that the n-type ZnSe layer, not the two n+ layers, in Wen corresponds to the semiconductor layers recited in independent claim 15. The n-type ZnSe layer in Wen does not comprise a plurality of semiconductor layers formed in spaced-apart relation in a surface of the semiconductor substrate, as required by independent claim 15. Since the n-type ZnSe layer in Wen does not have the specific structure of the semiconductor layers recited in independent claim 15, Wen clearly does not disclose or describe that an interface level region of the surface of the semiconductor substrate does not exist between the semiconductor layers, as required by independent claim 15.

The Examiner contends that Wen follows "exactly the same procedure" (e.g., wet etching) as described in the specification of the present invention in order to achieve the removal of the interface level region of the semiconductor substrate between the semiconductor layers. The Examiner therefore concludes that "the non-existence of an interface level region of the surface of the semiconductor substrate between the semiconductor layers" is "inherent in the device

as specified by" Wen. Applicant vigorously disagrees with this contention and with the Examiner's assertion of inherency to support this contention.

The Examiner's assertion that the feature "an interface level region of the surface of the semiconductor substrate does not exist between the semiconductor layers" in claim 15 is "inherent" in Wen is misplaced because such feature is not necessarily present in Wen. As stated by the Federal Circuit in Continental Can Co. USA v. Monsanto Co., 20 USPQ2d 1746, 1749-50 (Fed. Cir. 1991):

> To serve as an anticipation when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference and that it would be so recognized by persons of ordinary skill.

As recognized by the Examiner, Wen discloses the use of standard photolithography and wet etching techniques to implement the PIN photodiode. However, contrary to the Examiner's contention, such techniques are used to remove a portion in the area immediately above the n-type ZnSe layer (note the area denoted by arrow Y in Exhibit B) corresponding to the n+ layers, not the semiconductor layers (i.e., the n-type ZnSe layer in Wen). Thus the feature "an interface level

region of the surface of the semiconductor substrate does not exist between the semiconductor layers" recited in claim 15 is not present in Wen, and one of ordinary skill in the art would not recognize such feature to be present.

In the absence of the foregoing disclosure recited in independent claim 15, anticipation cannot be found. See, e.g., W.L. Gore & Associates v. Garlock, Inc., 220 USPQ 303, 313 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984) ("Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration"); Continental Can Co. USA v. Monsanto Co., 20 USPQ2d 1746, 1748 (Fed. Cir. 1991) ("When more than one reference is required to establish unpatentability of the claimed invention anticipation under § 102 can not be found".); Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 221 USPQ 481, 485 (Fed. Cir. 1984) (emphasis added) ("Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim").

Stated otherwise, there must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention. This standard is clearly not satisfied by Wen for the reasons stated above. Furthermore, Wen does not suggest

the claimed subject matter and, therefore, would not have motivated one skilled in the art to modify Wen's PIN photodiode to arrive at the claimed invention.

Claim 16 depends on and contains all of the limitations of independent claim 15 and, therefore, distinguishes from the reference at least in the same manner as claim 15.

In view of the foregoing, applicant respectfully requests that the rejection of claims 15-16 under 35 U.S.C. §102(b) as being anticipated by Wen be withdrawn.

Rejection Under 35 U.S.C. §103(a)

Claims 1-7 were rejected under 35 U.S.C. §103(a) as being unpatentable over Wen in view of APD. Applicant respectfully traverses this rejection and submits that the combined teachings of Wen and APD do not disclose or suggest the subject matter recited in independent claim 1 and dependent claims 2-7.

Independent claim 1 is directed to a photodiode and requires an optical detection portion for detecting an optical signal and outputting a photoelectric conversion signal, the optical detection portion having a semiconductor substrate of a first conductive type, a plurality of semiconductor layers of a second conductive type formed in spaced-apart relation in a surface of the semiconductor substrate, and a depletion

layer formed in the semiconductor substrate by application of a reverse bias to the photodiode so as to surround the semiconductor layers. Independent claim 1 further requires that the depletion layer has an etched surface portion disposed between the semiconductor layers so that an interface level region of the surface of the semiconductor substrate does not exist between the semiconductor layers. No corresponding structural combination is disclosed or suggested by the prior art of record.

The primary reference to Wen discloses a PIN photodiode as set forth above for the rejection of claims 15-16 under 35 U.S.C. §102(b). In the statement of rejection, the Examiner contends that the P-Si substrate and the n-type ZnSe layer in Wen correspond to the semiconductor substrate in independent claim 1 and that the n+ layers (i.e., ohmic contacts) correspond to the semiconductor layers in independent claim 1. The Examiner further contends that a boundary between the portion of the n+ layers that has been etched away and the n-type ZnSe layer corresponds to the etched surface portion recited in independent claim 1. Applicant respectfully disagrees with the Examiner's contentions and with the Examiner's interpretation of Wen in the rejection of the claims.

Wen does not disclose or describe a plurality of semiconductor layers formed in spaced-apart relation in a surface of the semiconductor substrate, as recited in independent claim 1, as set forth above for the rejection of claims 15-16 under 35 U.S.C. §102(b). Contrary to the Examiner's contention, one of ordinary skill in the art would recognize that the n-type ZnSe layer, not the two n+ layers, in Wen corresponds to the semiconductor layers recited in independent claim 1. The n-type ZnSe layer in Wen does not comprise a plurality of semiconductor layers formed in spaced-apart relation in a surface of the semiconductor substrate, as required by independent claim 1.

Wen also does not disclose or suggest a depletion layer having an etched surface portion disposed between the semiconductor layers so that an interface level region of the surface of the semiconductor substrate does not exist between the semiconductor layers, as required by independent claim 1. While acknowledging that neither Wen nor APD specifically teaches this structural feature recited in independent claim 1, the Examiner contends that this feature "follows from the device specification" of Wen because Wen follows "exactly the same procedure" (e.g., wet etching) as described in the specification of the present invention to achieve the removal of the interface level region of the semiconductor substrate

between the semiconductor layers. Applicant vigorously disagrees with the Examiner's contention.

As recognized by the Examiner, Wen discloses the use of standard photolithography and wet etching techniques to implement the PIN photodiode. However, contrary to the Examiner's contention, such techniques are used to remove a portion in the area immediately above the n-type ZnSe layer (note the area denoted by arrow Y in Exhibit B) corresponding to the n+ layers, not the depletion layer. Stated otherwise, the etched surface portion in Wen corresponds to the n+ layers, not the depletion layer in the n-type ZnSe layer in Wen. Thus, the depletion layer in Wen clearly does not have an etched surface portion and, more specifically, an etched surface portion disposed between semiconductor layers formed in spaced-apart relation in a surface of a semiconductor substrate, and that an interface level region of the surface of the semiconductor substrate does not exist between the semiconductor layers, as required by independent claim 1.

Moreover, even if the structure of the PIN photodiode disclosed by Wen is interpreted in the manner proposed by the Examiner, applicant respectfully submits that the resulting structure does not meet the limitations required by independent claim 1. More specifically, independent claim 1 requires that the depletion layer has an etched surface

portion disposed between the semiconductor layers so that an interface level region of the surface of the semiconductor substrate does not exist between the semiconductor layers. While Wen discloses that the n+ layers have an etched surface portion, as discussed above, there is no disclosure or suggestion that the exposed surface of the n-type ZnSe layer (corresponding to the surface of the semiconductor substrate of independent claim 1 in accordance with the Examiner's interpretation) has been etched away. Thus, even by the Examiner's interpretation, the resulting structure of Wen would at best correspond to the structure of the conventional photodiode shown in APD (Fig. 3), where the interface level region of the semiconductor substrate has not been removed.

Moreover, as recognized by the Examiner, Wen does not disclose or suggest a depletion layer formed in the semiconductor substrate by application of a reverse bias to the photodiode so as to surround the semiconductor layers, as recited in independent claim 1. With respect to this feature, the Examiner cited APD for its disclosure of a photodiode having a depletion layer surrounding semiconductor layers. The Examiner contends that it would have been obvious to one of ordinary skill in the art to modify Wen's photodiode to incorporate this structural feature taught by APD in order to further the purpose of Wen in increasing the sensitivity of

the phototiode. Applicant respectfully disagrees with the Examiner's contention.

It is unclear how the Examiner proposes to modify Wen in view of APD so that the depletion layer surrounds the semiconductor layers in Wen as interpreted by the Examiner (i.e., the n+ layers). Nevertheless, as discussed above, one of ordinary skill in the art would recognize the n-type ZnSe layer, not the n+ layers, as corresponding to the semiconductor layers in Wen. There is nothing in the references that would expressly or implicitly teach or suggest the modification urged by the Examiner and, therefore, the references do not directly establish this obviousness.

Thus one of ordinary skill in the art would not have been led to modify Wen in view of APD in the manner proposed by the Examiner in the statement of rejection. The only basis for the modifications urged by the Examiner in the rejection is applicant's own disclosure, and such hindsighted rejections are improper. See, for example, Diversitech Corp. v. Century Steps, Inc., 7 USPQ2d 1315, 1318 (Fed. Cir. 1988); In re Geiger, 2 USPQ2d 1276, 1278 (Fed. Cir. 1987); Panduit Corp. v. Dennison Manufacturing Co., 227 USPQ 337, 343 (Fed. Cir. 1985); Interconnect Planning Corp. v. Feil, 227 USPQ 543, 551 (Fed. Cir. 1985).

In order to support a claim rejection based upon obviousness under 35 U.S.C. §103, the Examiner must provide an evidentiary basis establishing the obviousness of each modification. The Examiner may do this by citing a reference which directly establishes this obviousness, or, the Examiner may otherwise set forth a line of reasoning consistent with and motivated by the cited art establishing that such modifications would have been obvious. Mere speculation or conclusory allegations are simply inadequate to meet this burden. There must be some teaching, reason, suggestion, or motivation found in the prior art references to make a combination which renders an invention obvious within the meaning of 35 U.S.C §103. See, e.g., Symbol Technologies, Inc. v. Opticon, Inc., 935 F.2d 982, 989, 18 USPQ2d 1885 (Fed. Cir. 1991).

In order to set forth a prima facie case of obviousness, the Examiner must not only demonstrate that this teaching exists in the prior art, but that it would teach all limitations of the claim. This burden cannot be met by citing references that, even if combined, fail to teach explicitly recited limitations.

Stated otherwise, in rejecting a claim as obvious under 35 U.S.C. §103, the Examiner cannot simply rely on a combination of references that teach some limitations of the

claim, and make mere conclusory allegations that the combination teaches others as well.

In the instant case, the Examiner has not met his burden of establishing a prima facie case of obviousness as discussed above.

As noted by the Court of Appeals for the Federal Circuit in the case of In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992):

> 'Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination. Under section 103, teachings of references can be combined only if there is some suggestion or incentive to do so.' Although couched in terms of combining teachings found in the prior art, the same inquiry must be carried out in the context of a purported obvious 'modification' of the prior art. The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. Wilson and Hendrix fail to suggest any motivation for, or desirability of, the changes espoused by the Examiner and endorsed by the Board.
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> Here, the Examiner relied upon hindsight to arrive at the determination of obviousness. It is impermissible to use the claimed invention as an instruction manual or 'template' to piece together the teachings of the prior art so that the claimed invention is rendered obvious. This court has previously stated that '[o]ne cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention.'

As further noted by the Federal Circuit in In re Oeticker, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992):

> The prima facie case is a procedural tool of patent examination, allocating the burdens of going forward as between examiner and applicant. In re Spada, 911 F.2d 705, 707 n.3, 15 USPQ2d 1655, 1657 n.3 (Fed. Cir. 1990). The term 'prima facie case' refers only to the initial examination step. In re Piasecki, 745 F.2d1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984); In re Rinehart, 531 F.2d 1048, 1052, 189 USPQ 143, 147 (CCPA 1976). As discussed in In re Piasecki, the examiner bears the initial burden, on review of the prior art or on any other ground, of presenting a prima facie case of unpatentability. If that burden is met, the burden of coming forward with evidence or argument shifts to the applicant.
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> If examination at the initial stage does not produce a prima facie case of unpatentability, then without more the applicant is entitled to grant of the patent. See In re Grabiak, 769, F.2d 729, 733, 226 USPQ 870, 873 (Fed. Cir. 1985); In re Rinehart, supra.
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> In reviewing the examiner's decision on appeal, the Board must necessarily weigh all of the evidence and argument. An observation by the Board that the examiner made a prima facie case is not improper, as long as the ultimate determination of patentability is make on the entire record. In re Piasecki, 745 F.2d at 1472, 223 USPQ at 788; In re Rinehart, 531 F.2d at 1052, 189 USPQ at 147.

The Federal Circuit has therefore made it clear that the prior art must show an incentive to modify its teachings

in order to render a claim obvious. Without such an incentive, a prima facie case of obviousness cannot be made.

Similarly, as the Board stated in Ex Parte Clapp, 227 USPQ 972, 973 (BPAI 1985):

> To support the conclusion that the claimed combination is directed to obvious subject matter, either the references must expressly or impliedly expound the modifications urged by the examiner to have been obvious.

The same situation exists here. The Examiner has not provided an evidentiary basis establishing the obviousness of his proposed modification of Wen. There is nothing in the reference to Wen or APD that would expressly or implicitly teach or suggest the modifications urged by the Examiner and, therefore, the references do not directly establish this obviousness. Furthermore, the Examiner has not set forth a line of reasoning consistent with and motivated by the cited art establishing that such modifications would have been obvious. Again, the only basis for the modifications urged by the Examiner in the rejection is applicant's own disclosure, and such hindsighted rejections are improper.

Claims 2-7 depend on and contain all of the limitations of independent claim 1 and, therefore, distinguish from the references at least in the same manner as claim 1.

Moreover there are separate grounds for patentability of several of the dependent claims.

Claim 2 includes the additional limitation that a distance between the semiconductor layers is 0.5 to 2 times a width of the depletion layer. Claims 4-7 are directed to the specific conductivity types of the semiconductor substrate and the semiconductor layers. To support its conclusion of obviousness, the Examiner has taken official notice that the selection of the specific distance between the semiconductor layers recited in claim 2 would be recognized by one of ordinary skill in the art. The Examiner has also taken official notice that since the selection of the specific conductivity types of the semiconductor substrate and the semiconductor layers "is fully standard in the semiconductor device art", no patentable weight should be given to the specific conductivity types recited in claims 4-7. Applicant respectfully disagrees with the Examiner's reliance on only officially noticed facts to support the conclusion that it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide semiconductor layers disposed at a distance of 0.5 to 2 times a width of the depletion layer, and to select the specific conductivity types recited in claims 4-7 for the semiconductor substrate and the semiconductor layers.

Applicant respectfully submits that officially noticed facts may only play a minor role in filling

evidentiary gaps to support a conclusion of obviousness and cannot provide the totality of evidence to support an obviousness rejection. In re Ahlert, 165 USPQ 418, 421 (CCPA 1970). See, also, In re Kaplan, 229 USPQ 678, 683 (Fed. Cir. 1986) ("Even if obviousness of the variation is predicated on the level of skill in the art, prior art evidence is needed to show what that level of skill was.").

In this case, the Examiner has failed to establish a recognition in the prior art, and thus knowledge thereof, of providing semiconductor layers disposed at a distance of 0.5 to 2 times a width of the depletion layer, as recited in claim 2, and the selection of the specific conductivity types recited in claims 4-7 for the semiconductor substrate and the semiconductor layers. Thus the Examiner cannot properly rely on a conclusion of obviousness solely on official notice to modify Wen as set forth in the Office Action to arrive at the invention recited in claims 2 and 4-7.

In view of the foregoing, applicant respectfully requests that the rejection of claims 1-7 under 35 U.S.C. §103(a) as being unpatentable over Wen in view of APD be withdrawn.

In view of the foregoing amendments and discussion, the application is believed to be in allowable form.

Accordingly, favorable reconsideration and allowance of the claims are most respectfully requested.

Respectfully submitted,

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